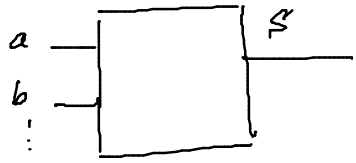
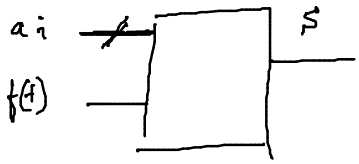
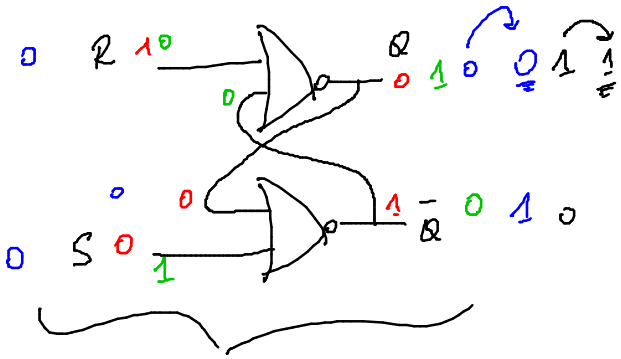
Séquence 2 — A12

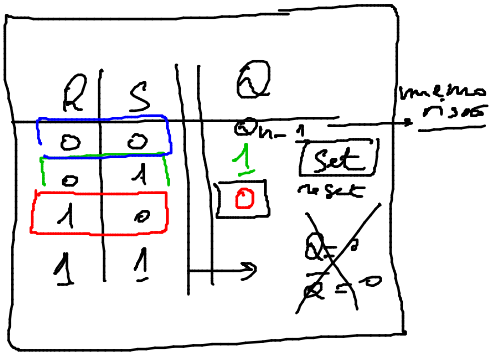
Logique combinatoire → logique séq M_s.

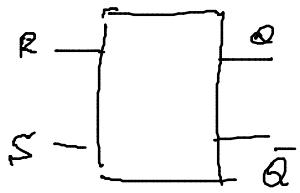




L'élt de base — bascule

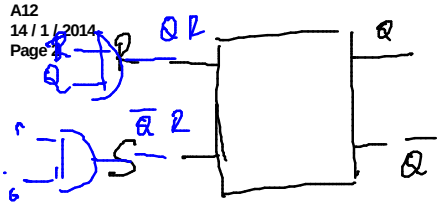


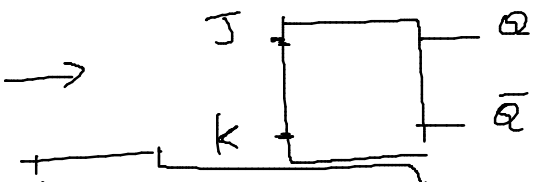




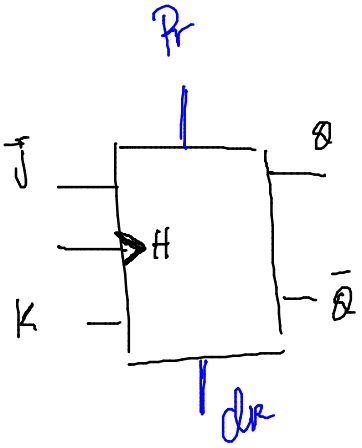
$Q=0 \rightarrow Q_{n+1} = 0$

$Q=1 \rightarrow Q_{n+1} = 1$

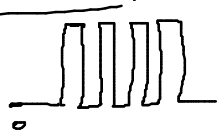


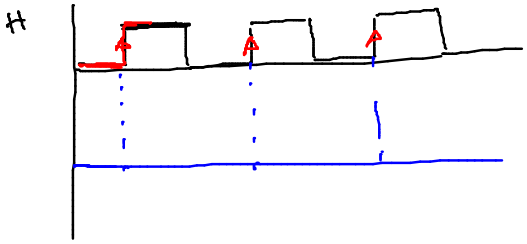


J	k	Q_n
0	0	Q_{n-1}
↑	0	1
0	↓	0
1	↓	$\overline{Q_{n-1}}$

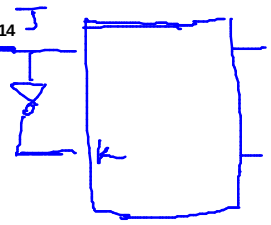


J = 1
k = 1



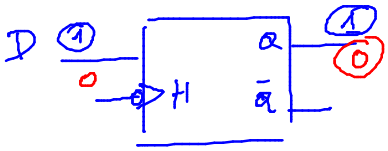


(Pr et clk) → entrées asynchrones prioritaires.



1 0
0 1

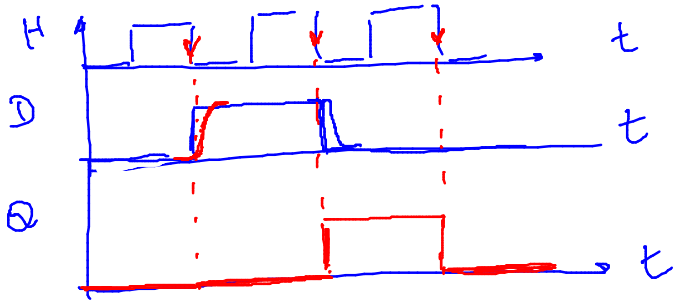
Bascule D.



Copie la valeur de D

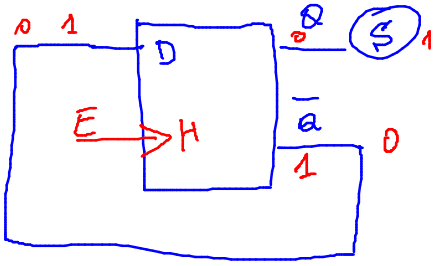
t_{PLH}

Rq



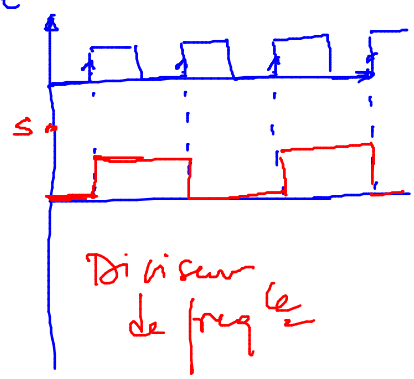
à $t=0$
$Q=0$

E / 1



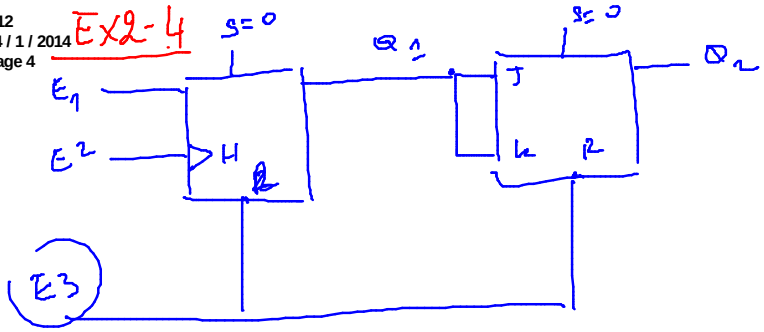
A $t=0$; $Q=0$

E

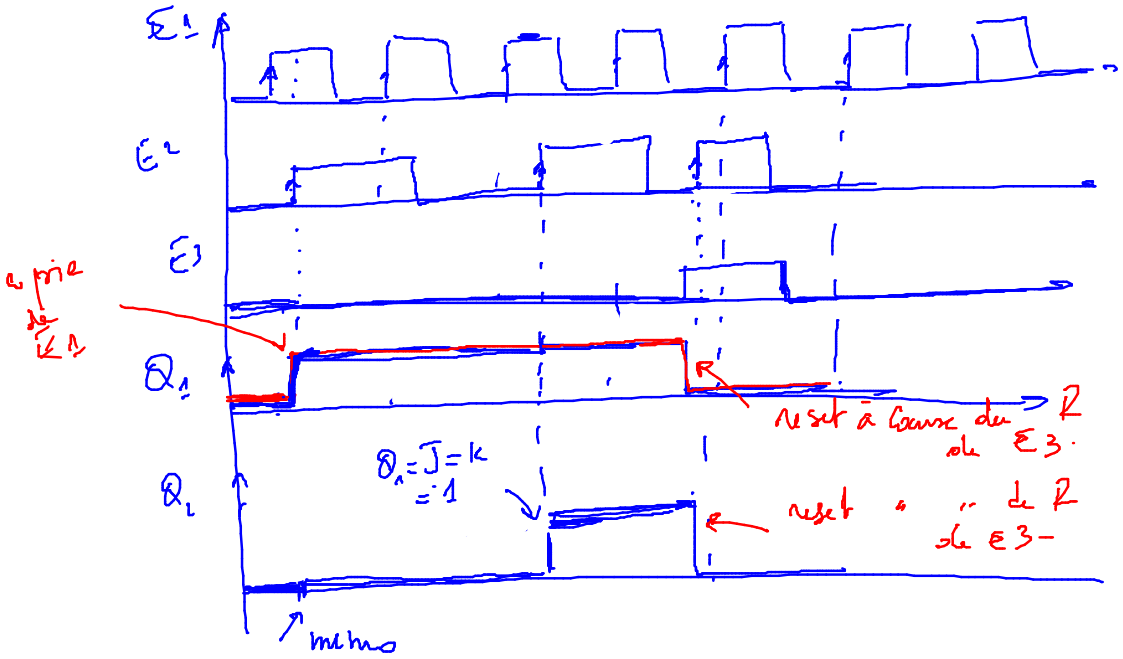


Diviseur de fréquence

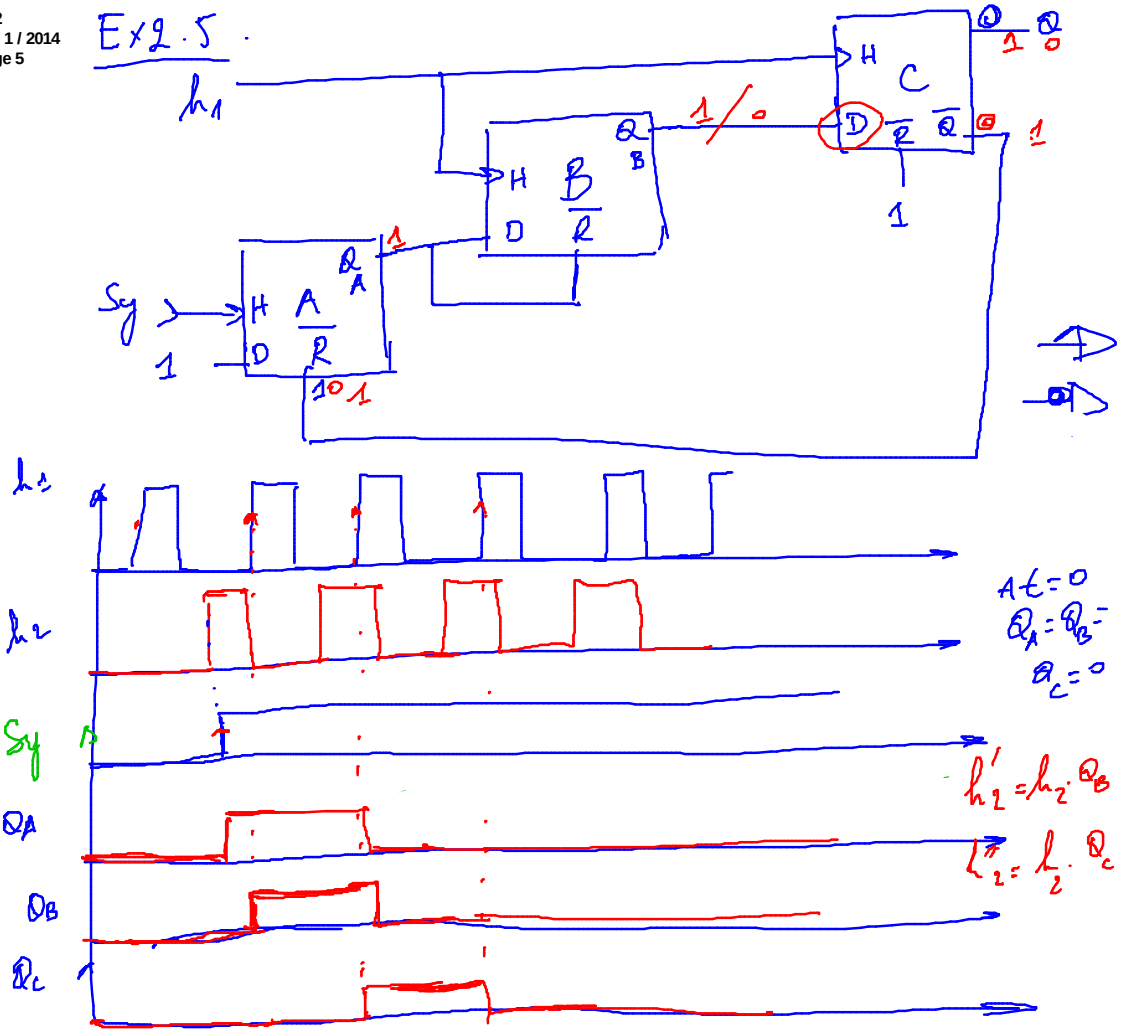
Ex2-4



(S=0, R=1) → reset

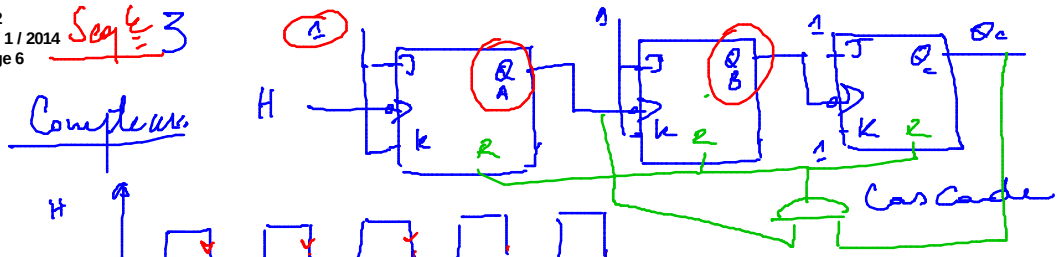


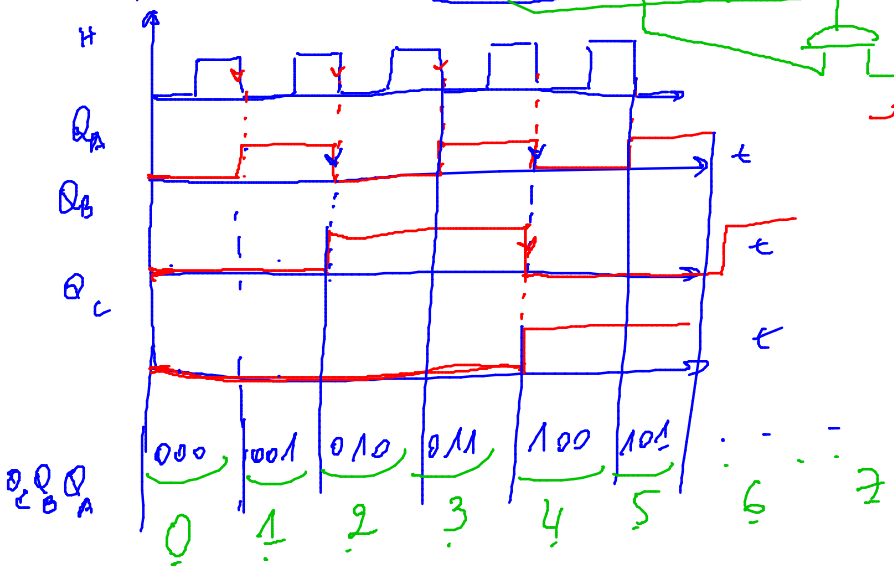
Ex 2.5


h1
H
C
D
R
Q
Q
1
0
H
B
D
R
Q
B
1/0
H
A
D
R
Q
A
Sy
1
1
0
1
1
h2
Sy
QA
QB
QC
At = 0
QA = QB = QC = 0
h'2 = h2 · QB
h''2 = h2 · QC

Seq 3

Compteur





A $t=0$

$Q_A = Q_B = Q_C = 0$

Compteur (Cascade) asynchrone

Décompteur / Modulo 8 états

3 bits

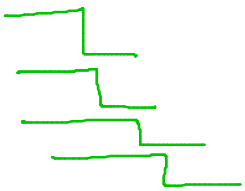
100
101
110
111

Compteur module 5 :

$Q_C Q_B Q_A$

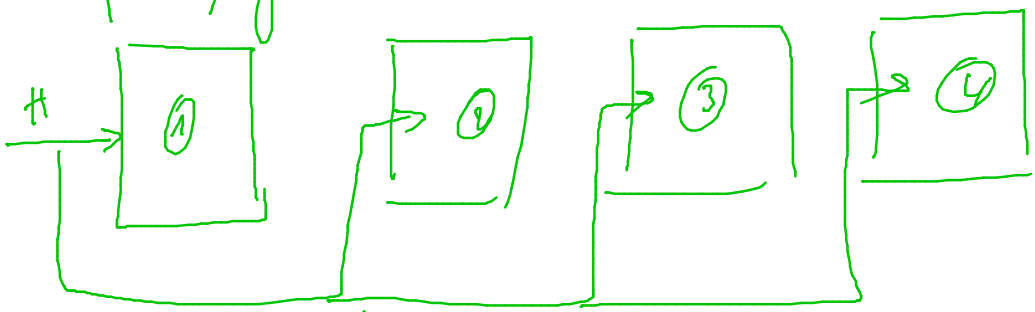
101 ←

Compteur asynchrone.



limites :

Compteur synchrone voir Ex. 3-1



Q_C	Q_B	Q_A	$J_A = K_A$	$J_B = K_B$	$J_C = K_C$
0	0	0	1	0	0
0	0	1	1	1	0
0	1	0	.	.	.
0	1	1	.	.	.
1	0	0	.	.	.
		.			
		:			

$J_A = 1 \quad K_A = 1$

$J_B = Q_0$

$J_C = Q_0 \, Q_1$

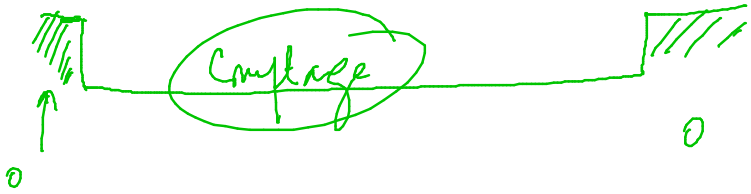
$J_D = Q_0 \, Q_1 \, Q_2$

Ex3. Système synchrone.

Q_3	Q_2	Q_1	Q_0	$J_0 = K_0$	$J_1 = K_1$	$J_2 = K_2$	$J_3 = K_3$
				1	Q_0	$Q_0 Q_1$	$Q_0 Q_1 Q_2$
→ 0	0	0	0	1	0	0	0 ←
0	0	0	1	1	1	0	0 ←
0	0	1	0	1	0	0	0 ←
0	0	1	1				
⋮							
1							

Ex3.1 : Compteur synch. modulo 16

RAZ.



Ex : 3_2

Diviseur de fréquence par 4.

2^2