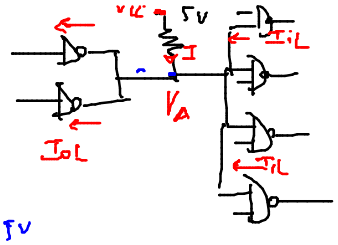
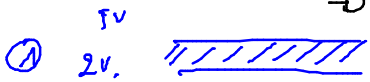
Le cours reprend

$V_A = V_{CC} - R\,I < 0{,}4\ V$

pour être comprise comme tension à l'état bas

Etat bas





$I + 4\,I_{iL} = 2\,I_{oL}$

$I = 2\,I_{oL} - 4\,I_{iL}$

$= 32\ mA - 4 \times 1{,}6\ mA$

Or si 1 seule porte fonctionne $\Rightarrow$ alors

$I = I_{oL} - 4\,I_{iL}$

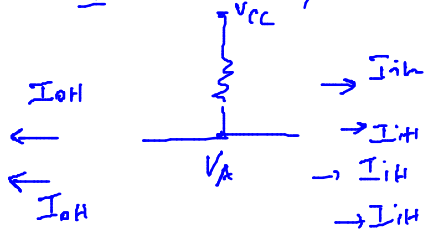
$= 16 - 6{,}4\ mA$

$= 9{,}6\ mA$

$V_A = V_{CC} - RI < 0{,}4$

$R > \dfrac{V_{CC} - 0{,}4}{I} = \dfrac{5 - 0{,}4}{9{,}6 \cdot 10^{-3}} \approx 480\ \Omega$

Etat haut



$V_A > V_{IH\,min}$

$I = 2\,I_{oH} + 4\,I_{oH}$

$V_A = V_{CC} - RI > V_{IH\,min} = 2V$

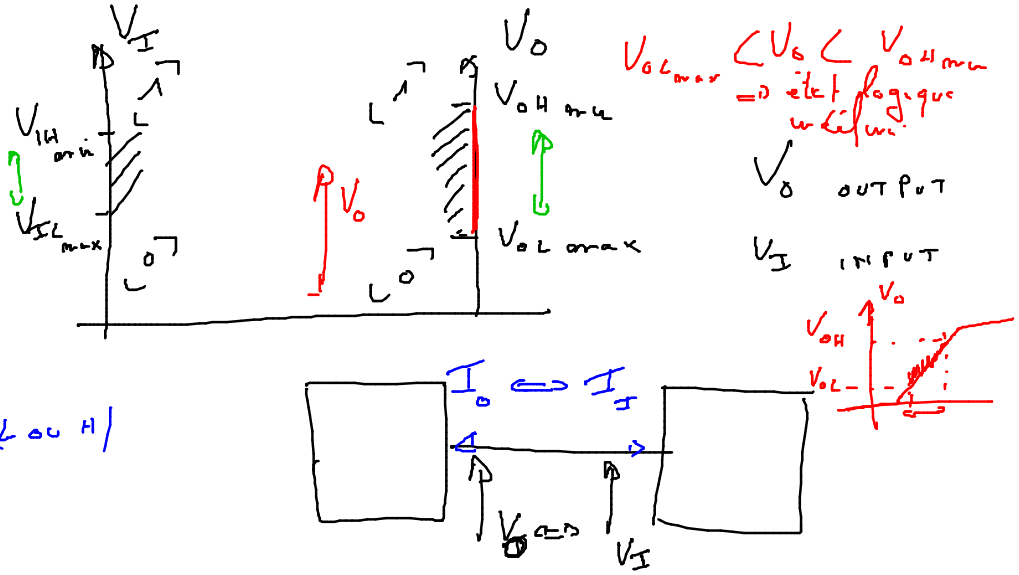
$R < \dfrac{5 - 2}{660 \cdot 10^{-6}} = 4{,}5\ k\Omega$

$480\,\Omega < R < 4{,}7\,k\Omega \Rightarrow$ $R = 2{,}5\,k\Omega$

Rq : de le cas en Etat bas.

Séquence 5

→ plusieurs paramètres pour interfaçage
- niveau de tension
- niveau de courant (sortie)
- puissance, temps de propa (fréq.)



$V_{OL\ max} < V_O < V_{OH\ min}$ ⇒ état logique indéfini

V_O OUTPUT

V_I INPUT

$I_{O(L\ ou\ H)}$

Ex 5.5

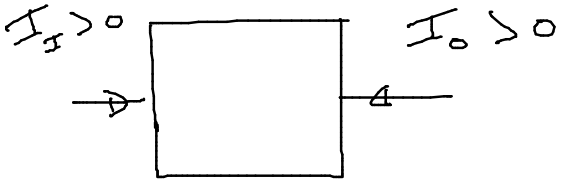
p°81 polycopié → V / I pour TTL, CMOS

Définition des sens des courants en TTL

74 TTL par ex.

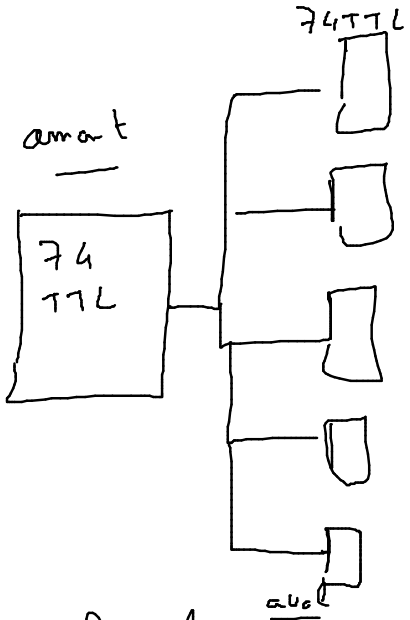
$I_{IH} = +40\ \mu A$ $\qquad$ $I_{OH} = -0{,}4\ mA$

$I_{IL} = -1{,}6\ mA$ $\qquad$ $I_{OL} = +16\ mA$



Courant entrant > 0

Courant sortant < 0



Si on famille de CI ⇒ compatibilité assurée en tension
⇒ Sortance

$$\text{Sortance} = \min\left(\frac{I_{OH}}{I_{IH}} ; \frac{I_{OL}}{I_{IL}}\right)$$

74 TTL

$$\text{Sortante} = \min\left(\frac{0{,}4\ \text{mA}}{40\ \mu\text{A}}\ ;\ \frac{16\ \text{mA}}{1{,}6\ \text{mA}}\right)$$

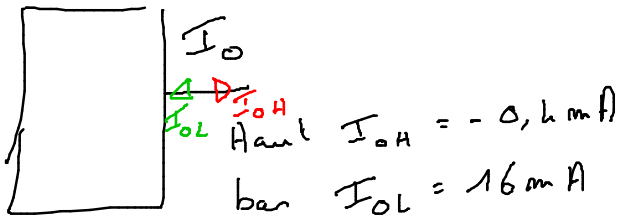
$\uparrow$ haut $\quad\uparrow$ bas

$$= \min(10\ ;\ 10) = 10 > 5$$

$\Rightarrow$ circuit (OK)

((niveau haut, porte aval débite 0,4 mA
niveau bas, porte aval absorbe 16 mA

$\uparrow$ TTL NON ET



haut $I_{OH} = -0{,}4$ mA

bas $I_{OL} = 16$ mA

5.1

1) Consommation : $P = U \cdot I$

2) $P_{Haut} = V_{alim} \cdot I_H = 7 \cdot 10^{-3} \times 15$
$= 105\ mW$

$P_{Bas} = V_{alim} \cdot I_L = 4 \cdot 10^{-3} \times 15$
$= 60\ mW$

3) rapport cyclique 50 %

$P = \frac{1}{2} (P_{Haut} + P_{Bas}) = 82,5\ mW$

$= \frac{1}{2} P_H + \frac{1}{2} P_B$

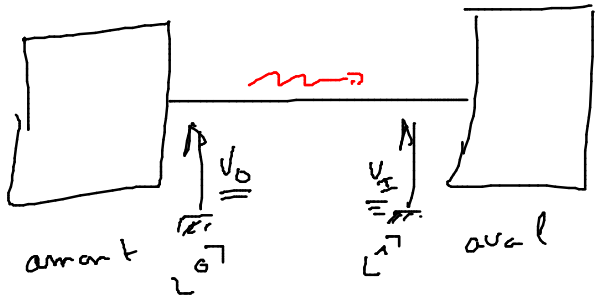
5.3

4) compromis vitesse/conso → facteur de mérite

= retard de propagation × consommation

5.4.1 Marge de sensibilité aux bruits :

TTL-LS



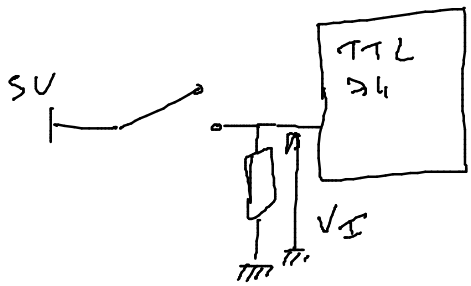
Haut

$V_{H\,(H)} = V_{OH} - V_{IH} = 2,7 - 2 = 0,7\,V$

Bas

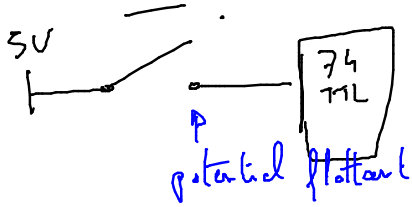
$V_{H\,(L)} = |V_{OL} - V_{IL}| = V_{IL} - V_{OL} = 0,8 - 0,5 = 0,3\,V$

5.2



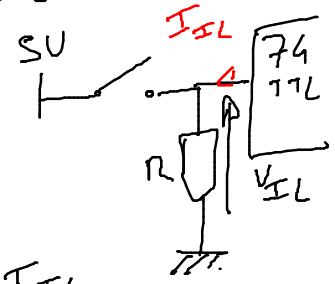
1) Haut : $(V_{I+1})_{min} = 2,0\,V$ → interrupteur fermé
→ $5V = V_I$
$5V > 2V$
L → OK

Bas ? → interrupteur ouvert



potentiel flottant

V_I ??



$V_{IL} = R \cdot I_{IL}$

$$R = \frac{(V_{IL})_{max}}{(I_{IL})_{max}} = \frac{0,8}{1,6\,mA} = 500\,\Omega$$

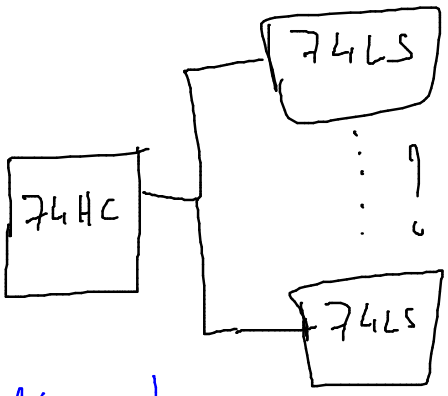
2.) TTL LS

$$R = \frac{(V_{IL})_{max}}{(I_{IL})_{max}} = \frac{0,8}{0,4\,mA} = 2k\,\Omega$$

Séquence 6

6.3

1°)



a) → compatibilité en tension

b) → sortance

a)

	74HC		74LS
Haut	V_{OH} min = 4,9 V	>	V_{IH} min = 2,0 V
Bas	V_{OL} max = 0,1	<	V_{IL} max = 0,8 V

OK

b) $Sortance = \min\left(\frac{I_{OH}}{I_{IH}}, \frac{I_{OL}}{I_{IL}}\right)$

$= \min\left(\frac{4\,mA}{20\,\mu A}; \frac{4\,mA}{0,4\,mA}\right)$

$= \min(200; 10) = 10$

$\Rightarrow$ max 10 portes 74LS pilotables par 1 HC

2°) Sortie 4000B qui pilote un porte 74LS compatibilité en tension

$V_{OH\,min}(4000B) = 4,95V > 2V$

$V_{OL\,max}(4000B) = 0,05V < 0,8V$ } (LS)

$\Rightarrow$ (OK)

Sortance = min (0,4 mA / 20 µA , 0,4 mA / 0,4 mA)

= min (20 , 1) = 1

1 seule porte 4000 B → 1 seule porte 74LS

3) → pas de pb pour la compatibilité en tension

→ sortance = min (4 mA / 200 µA ; 4 mA / 2 mA) = 2 ⚠

1 HC → 2 portes max. 74AS

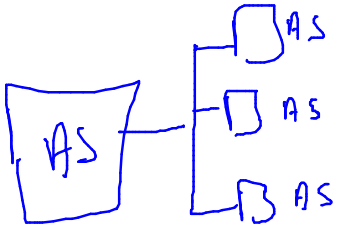
(pb)

Solutions
- charger les 3 portes AS par des LS
- charge la porte HC pour AS

AS ⇒ AS

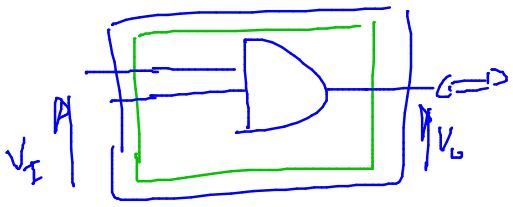
Sortanca = min(2mA / 200μA ; 20mA / 2mA)

= min (10, #ho) = 10

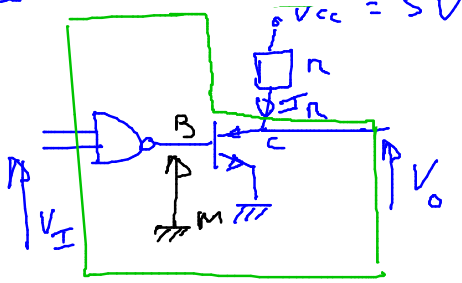


6.2

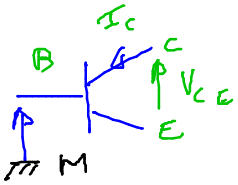
① porte ET à collecteur ouvert

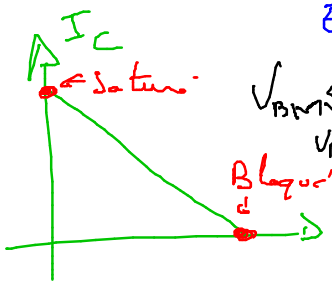


ET



ET





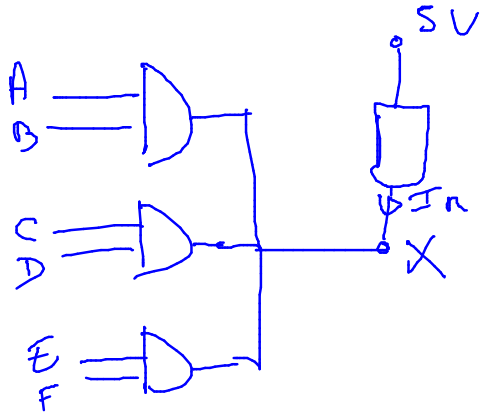
$V_{BM} < 0 \Rightarrow$ Bloqué $I_c \neq 0$

$V_{BM} > 0$ Saturé $I_c \neq I_{Cmax} = I_{Csat}$

Sortie de NOM ET → Base du transistor

- $V_I = V_{IH} \rightarrow V_{BM} = V_{OL} = L^0 \Rightarrow$ Blocage $I_c = 0 \Rightarrow I_R = 0$
- $V_I = V_{IL} \rightarrow V_{BM} = V_{OH} = 1$ $\Rightarrow$ saturation ; I_{cmax} $V_o = V_{cc} = 5V$ $V_o = V_{cc} - R I_{cmax} = L^0$

a) X =



- quand X = 5V ?
  s. $I_R = 0$ A
  s. 3 transistors sont bloqués

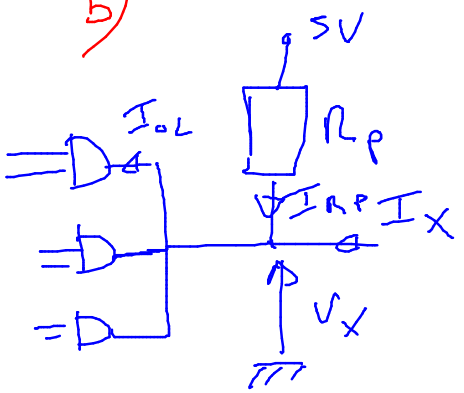
$A.B.C.D.E.\overline{F} = 1$

- s. 1 seul (au moins) est saturé $\Rightarrow I_{C_{sat}} = I_R$
  $\Rightarrow X \neq 5V$

1 des 6 entrées vaut 0 $\Rightarrow$ X = 0

$X = A.B.C.D.E.\overline{F}$

b)



Etat bas en sortie

$(V_{OL})_{TTL}$

$\Rightarrow$ (4 portes TTL)

$I_4 = 4 \times 1,6\,mA$

$= 6,4\,mA$

$5 - V_X = R_{RP} I_{RP}$

$I_{RP} + I_X = I_{OL}$

$\Rightarrow \boxed{R_p = \dfrac{5 - V_X}{I_{RP}} = \dfrac{5 - V_X}{I_{OL} - I_X}}$: $\dfrac{5 - 0,4}{30\,mA - 6,4\,mA}$

$V_X = (V_{OL})_{TTL}$

$I_{OL} = 30\,mA$

$V_{OL} = 0,4\,V$

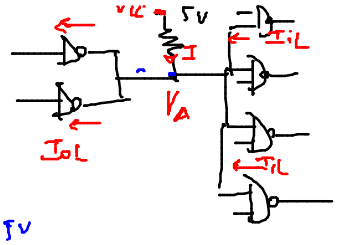
$R_p = 195\,\Omega$

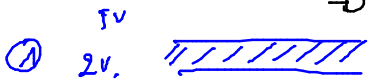
Le cours reprend

$V_A = V_{CC} - R\,I < 0{,}4\ V$

pour être comprise comme tension à l'état bas

Etat bas





$I + 4\,I_{iL} = 2\,I_{oL}$

$I = 2\,I_{oL} - 4\,I_{iL}$

$= 32\ mA - 4 \times 1{,}6\ mA$

Or si 1 seule porte fonctionne $\Rightarrow$ alors

$I = I_{oL} - 4\,I_{iL}$

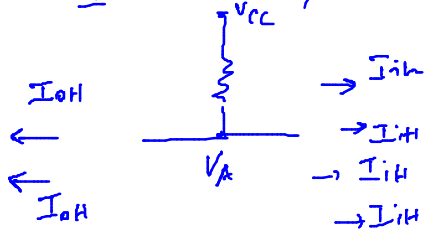
$= 16 - 6{,}4\ mA$

$= 9{,}6\ mA$

$V_A = V_{CC} - RI < 0{,}4$

$R > \dfrac{V_{CC} - 0{,}4}{I} = \dfrac{5 - 0{,}4}{9{,}6 \cdot 10^{-3}} \approx 480\ \Omega$

Etat haut



$V_A > V_{IH\,min}$

$I = 2\,I_{oH} + 4\,I_{oH}$

$V_A = V_{CC} - RI > V_{IH\,min} = 2V$

$R < \dfrac{5 - 2}{660 \cdot 10^{-6}} = 4{,}5\ k\Omega$

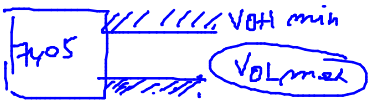
$480\,\Omega < R < 4{,}7\,k\Omega \Rightarrow R = 2{,}5\,k\Omega$

Rq : dans le cas où Etat bas $\Rightarrow$ =

$R > \frac{V_{CC} - 0{,}4V}{I}$

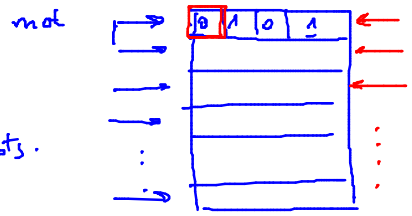
$R > \frac{V_{CC} - 0}{I} = 520\,\Omega$

Contrainte plus forte



Séquence 7

7.1 16k x 32



1°) Nbre de mots $16 \times 1024 = 16384$ mots.

2°) Nbre de bits par mot : 32

3°) $16384 \times 32 = 524288$ Cellule mémoire.

4°) Nbre d'adresses : 16384 adresses.

5°) bits d'adresses / lignes d'adresses

$2^N = 16384 \Rightarrow \boxed{N = 14}$

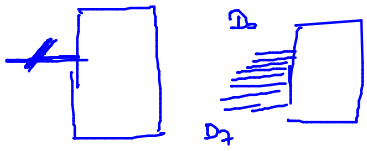
$A_1 A_0$: 00 → 01 → 10 → 11 →

$\boxed{A_{13} A_{12} \ldots\ldots A_0}$

7.2 4k x 8

mots 8 bits

4k mots



1°) 8 entrées de data car mots de 8 bits.

2°) $2^N = 4k = 4 \times 1024 = 4096$ $\boxed{N = 12}$ lignes d'adresse.

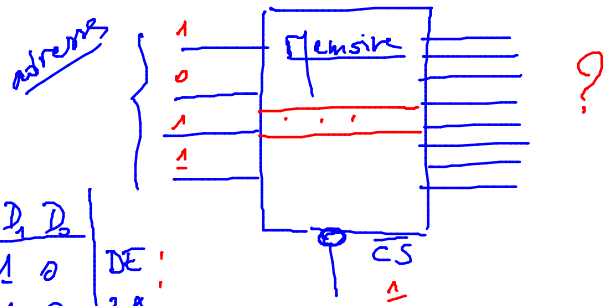
3°) Capacité : 4k octets

$\log 2^N = \log 4096$

$N \log 2 = \log 4096$.

$A_{11} A_{10} A_9 \ldots A_0$

7.3



D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1	1	0	1	1	1	1	0	DE
0	0	1	1	1	0	1	0	3A
1	0	0	0	0	1	0	1	95
1	1	1	0	1	1	0	1	ED

[A] : 1011

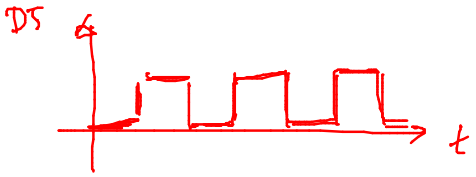
1°/ sortie haute impédance

2°/ [A] 0111 , $\overline{CS} = 0$.

→ ED en sortie

1110 1101.

3°/ 0000
0001
0010
.
.



Ex-7.4

4k * 8.

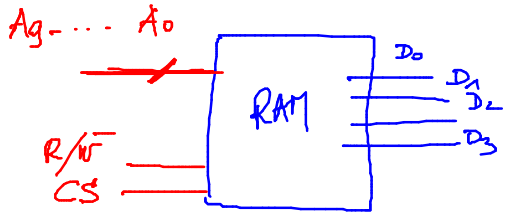
a) 8 entrées / sorties de data.

b) 12 lignes d'adresses.

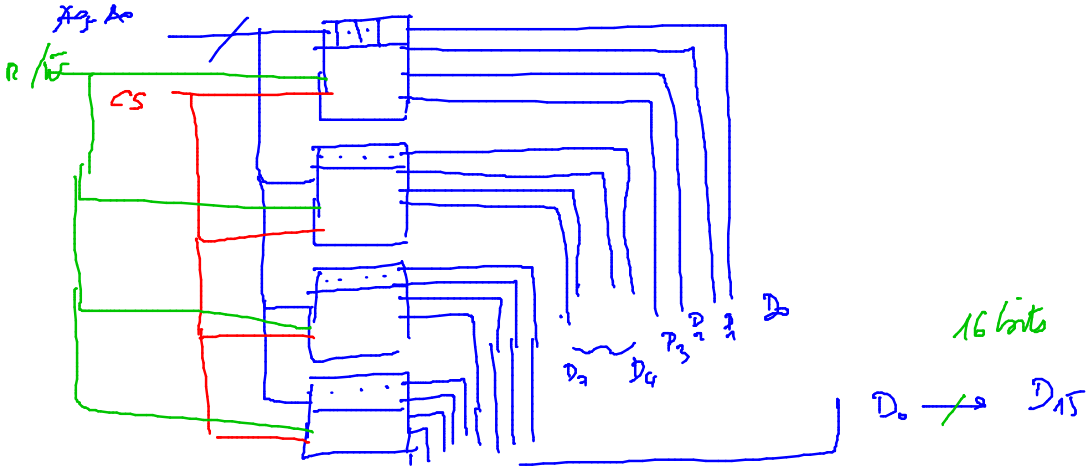
Séquence 8-1

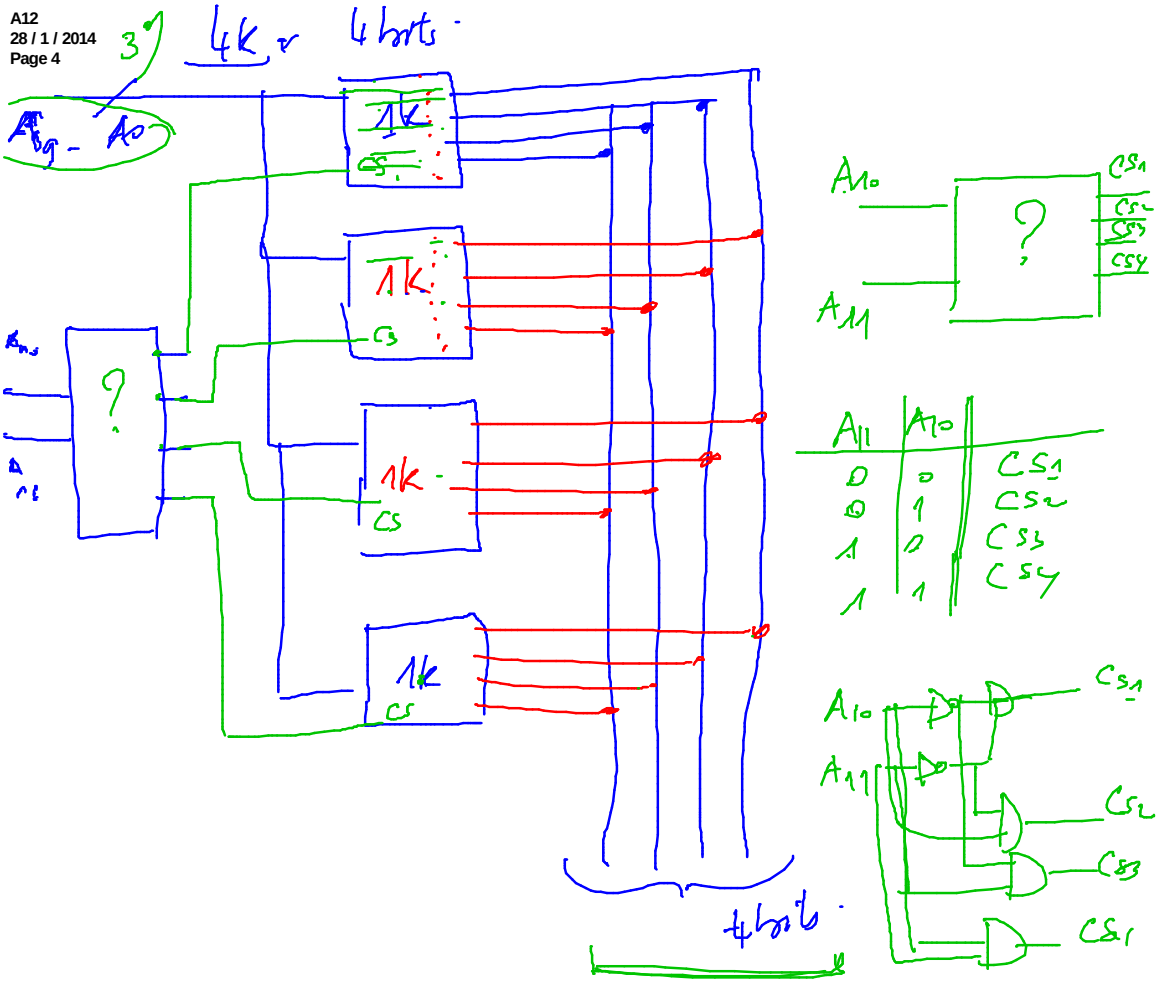
1°) RAM 1k * 4 bits

$2^N = 1024 \Rightarrow$ | N = 10 |



2°) 1k * 16 bits





A_{11}	A_{10}	
0	0	CS_1
0	1	CS_2
1	0	CS_3
1	1	CS_4